Substrates for GaN Technology

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Outline

View from technologists perspective

- do not expect a lot of crystallography

- What is GaN good for ?
- Why are substrates an issue ?
- Routes to defect reduction
- Routes to freestanding substrates
- Bulk GaN crystals
- Conclusions and outlook
Why GaN for optoelectronics?

Emission (and detection) wavelength/color

GaN/GaInN:
- direct semiconductor
- emission in near UV – blue – green region
  → LEDs, blue laser

AlGaN/GaN:
- emission/absorption in UV
  → UV-LEDs “solar blind” UV detectors

Applications in optoelectronics I

White light from
- light from blue LED mixed with secondary light from two phosphors
- UV LED for pumping of three phosphors

For
- LCD backlight
- general lighting
- automotive

Green traffic light
Applications in optoelectronics II

White and blue LEDs for displays

Data storage

BlueRay Disc
GaN - Laser @ 405 nm

Why GaN for electronics?

Potentially best performance for high power at high frequency
Material properties

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>4H SiC</th>
<th>6H SiC</th>
<th>GaN: AlGaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap (eV)</td>
<td>1.1</td>
<td>1.43</td>
<td>3.26</td>
<td>3.0</td>
<td>3.42</td>
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<tr>
<td></td>
<td>ind.</td>
<td>dir.</td>
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<tr>
<td>Electron mobility</td>
<td>1500</td>
<td>8500</td>
<td>1000</td>
<td>500</td>
<td>1250</td>
</tr>
<tr>
<td>(cm²/V.s)</td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Electric breakdown</td>
<td>0.3</td>
<td>0.4</td>
<td>2.0</td>
<td>2.4</td>
<td>3.3</td>
</tr>
<tr>
<td>field (10⁵ V/cm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Saturation velocity</td>
<td>1.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.7</td>
</tr>
<tr>
<td>(10⁷ cm/s)</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Thermal conductivity</td>
<td>1.5</td>
<td>0.46</td>
<td>4.9</td>
<td>4.9</td>
<td>1.3</td>
</tr>
<tr>
<td>(W/K cm)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Johnsons Figure of</td>
<td>1</td>
<td>7</td>
<td>180</td>
<td>260</td>
<td>760</td>
</tr>
<tr>
<td>Merit (~V_B x v_sat²)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Maximum estimated</td>
<td>200</td>
<td>300</td>
<td>500</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>operation temperature (°C)</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

High breakdown voltage + high saturation velocity  ➔ good power performance at high frequencies

GaN HFET (MODFET, HEMT)

Carriers transferred from AlGaN and/or GaN (due to spontaneous and piezoelectric polarization) to channel at interface

Conductivity of channel controlled by gate voltage / field

High breakdown voltage of GaN  ➔ high source-drain voltage possible  ➔ high power operation

GaN HBT still far from application
GaN HFET at FBH

Processed wafers on transparent SiC substrate

Packaged high power transistor

Applications in electronics

Power amplifiers for mobile communication, radio links, radar
Which GaN?

GaN device technology uses hexagonal wurtzite GaN with c-plane orientation.

Other orientations (nonpolar m-plane, a-plane for UV emitters) or polytypes (cubic zincblende) are research topics.

Growth methods – MOVPE

Metalorganic Vapour Phase Epitaxy

\[ \text{Ga(CH}_3\text{)}_3 + \text{NH}_3 \rightarrow \text{GaN} + 3 \text{CH}_4 \]

Typically at reduced pressure

Multiwafer reactors (49 x 2"

The method for mass production of LEDs

AIX 2600 HT 11x2“

at FBH
Growth methods – MBE

Molecular Beam Epitaxy

UHV

Ga from Knudsen cells

NH* or N* from plasma cracking of NH₃ or N₂

Primarily research tool:
Surface studies
Different polarities

Some device work primarily for GaN-HFETs

Growth methods – HVPE

Hydride vapour phase epitaxy

open hotwall reactor

HCl

GaCl, H

N₂

NH₃

Ga

Substrat

700-900 °C
Ga + HCl → GaCl + 1/2 H₂

900-1100°C
GaCl + NH₃ → GaN + HCl + H₂

GaN ↔ Ga + 1/2 N₂

Ga + NH₃ ↔ GaN + 3/2 H₂

Used for thick layers: growth rates above 100 µm/h demonstrated
AIX-HVPE at FBH

Reflectometry (LayTec EpiR) important tool for control of growth
Horizontal reactor with cross flow geometry (optimized together with Aixtron)
Research tool to understand growth and optimize technology

Substrates for GaN

- Si technology uses Si substrates
- GaAs technology uses GaAs substrates
- GaN technology waits for GaN substrates
  - currently uses
    - Sapphire (opto)
    - SiC (Si for electronics, n-type for opto)
    - some Si
    - GaN samples with very high prices
  - tries
    - AlN
    - LiAlO₂
    - ZrB₂
    - MgO
    - others
Substrate choice

Criteria:
- lattice coincidence
- lattice matching
- thermal expansion coefficient (TEC)
- surface chemistry
- temperature stability
- conductivity
  - thermal
  - electrical
- cleavability
  (laser diodes)
- availability
- price

Sapphire, SiC and Si

<table>
<thead>
<tr>
<th></th>
<th>α - (0001) Al₂O₃</th>
<th>SiC (6H, 4H)</th>
<th>Si (111)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Δa/a (%)</td>
<td>-13.8</td>
<td>-3.5</td>
<td>17 reduced by rotation</td>
</tr>
<tr>
<td>ΔTEC (1/K)</td>
<td>+1.7x10⁻⁶</td>
<td>-1.1x10⁻⁶</td>
<td>-2x10⁻⁶</td>
</tr>
</tbody>
</table>

Bowing direction for thin layers depending on growth process, tensile and compressive possible

- insulating
- SC: for opto
- SI: for electronics
- semiconducting

- cheap, up to 4”
- expensive (n-type)
- prohibitive (Si) (2,500€ for 2”)
- cheap (despite stange orientation)

- Most LEDs
- High thermal resistance

- HFET (SI)
- Some LED (n-type)
- Nanopipes
- HFET (Nitronex)
- LED research
- Dissolves in Ga
Substrate limitations I

Mismatch of lattice constant and thermal expansion coefficient

- dislocations: limit device performance (and lifetime) since they act as recombination and scattering centers
- bow: problem for device technology
  - sub-µm lithography difficult due to limited depth of focus
  - inhomogeneous thermal contact in epitaxy or plasma etching
  - polishing of larger areas / full wafer impossible
- cracks: render layers useless for devices

Dislocation density I

Blue (405 nm) laser diodes
Defect reduction by one order of magnitude yields
- reduced threshold current
- higher output power
- (higher reliability)

Data provided by
K. Köhler
Dislocation density II

Luminescence (PL and EL) efficiency drops with increasing defect density

Effect most severe for short (UV) and long (green) wavelength

Akita et al.; phys. stat. sol. a 201 (2004) 2624

Bow

Severe bowing with increasing layer thickness

For standard sapphire substrates (330 µm thick) minimum radius only – 40 cm!

No polishing possible

Inhomogenous thermal contact in device epi (wavelength shift in LEDs)

Stress partly released by cracks in GaN layer that can propagate into substrate
Cracking I

2" wafers GaN/sapphire from HVPE without cracks in the surface possible (here: 90 µm, 200 µm also demonstrated)

but

Dependent on starting layer and not necessarily stable

Cracking after cool-down or even after weeks of storage

Cracking II

90 µm thick layer with crack-free surface

Cracks close during growth depending on growth conditions

Increasing crack density towards substrate can move into substrate and cause breakage
Substrate limitations II

**Thermal conductivity**

Tenfold lower thermal conductivity of sapphire (0.3 W/cmK) in comparison to SiC (4 W/cmK) leads to:
- lower maximum current
- stronger current reduction at higher drain voltage / power

Heat dissipation important for power devices:
- transistors
- laser diodes
- LEDs!!

Drain current vs. drain voltage for GaN HFET on sapphire and SiC

Substrate limitations III

**Electrical conductivity**

LED on insulating sapphire requires two front contacts
- not matched with conventional LED technology

LED on conducting substrate (SiC) needs:
- nucleation / buffer layer has to be conductive

MODFET needs (semi)insulating substrate and high resistivity nucleation / buffer layer
Epi growers dream

Substrate

- for homoepitaxy
  - no worries with mismatch and delicate nucleation / buffer layer growth schemes
- with reasonable (for unipolar devices) or low (for bipolar devices) dislocation densities
- available as n-type (opto) or SI (electronics) (p-type would also be nice to have)
- at affordable prices (currently 2" Si:SiC 2,500 €!)

Substrate from classical bulk growth

- Si 300 mm x 2000 mm
  - www.msil.ab.psiweb.com (2001)
- GaAs 150 mm x 300 mm
  - www2.hitachi-cable.co.jp (2001)
- GaN 10 mm x 15 mm
  - S. Porowski, MRS IJNS, R4S1, G1.3 (1999)

HPSG ~15 kbar, ~1800 K
Thermodynamic limitations

N$_2$(g)-Ga(l)-GaN(s)- phase diagram and N$_2$ solubility in Ga

growth from melt would require 2800 K and > 45 kbar

S. Porowski, MRS IJNS, R4S1,G1.3 (1999)

High Pressure Solution Growth (HPSG)

Growth at 18 kbar

Crystals with good crystalline properties
(defect density < 10$^2$ cm$^{-2}$ claimed)

Used for device demonstration
(blue laser by MOVPE)

No breakthrough with respect to size
stagnant at 10 mm x 10 mm x < 0.5 mm
since years

Availability in 2” currently not foreseeable

Group of Sylvester Porowski
Institute of High Pressure Physics of the Polish Academy of Sciences
(IHPP PAS – Unipress) and spin-off Top Gan
Why are GaN substrates not (really) available?

Classical melt growth not feasible due to high N vapor pressure

HPSG demonstrated, but upscaling still open

Low pressure solution growth (liquid phase epitaxy) suffers from low solubility of N

- despite use of “solvents” only rates of the order of 1 µm/h
- not useful for bulk growth

Ammonothermal method (growth from precursors like Ga hydroxide, Ga nitrate ..., and NH₃) : only small crystallites

Sublimation growth: small needles (works for AlN)

- None of the classical bulk growth methods works (yet??)

Defect reduction in heteroepitaxy

Careful optimization of nucleation and buffer layer growth on sapphire or SiC

- Mid 10⁷ cm⁻² dislocation density is possible
- Still too high for laser diodes with high output power

Use of optimized substrate miscut: not well studied in literature but no reduction by orders of magnitude to be expected
Defect reduction via layer thickness

- Mutual annihilation of dislocations with increasing thickness
- High growth rates needed
- Hydride Vapour Phase Epitaxy


Defect reduction in heteroepitaxy

- Careful optimization of nucleation and buffer layer growth on sapphire or SiC
  - Mid $10^7$ cm$^{-2}$ dislocation density is possible
  - Still too high for laser diodes with high output power
- Use of optimized substrate miscut: not well studied in literature
- Increase layer thickness
  - Reduces defect density
  - Leaves problem of bow and cracks
Selective Area Growth (SAG)

Epitaxial Lateral Over Growth (ELOG)
Masked: patterned SiN or SiO₂
Maskless: porous SiN grown in-situ

Pendeo-Epitaxy (PE)

Reduction of dislocation density by bending and mutual annihilation

ELOG I
Defect reduction in area above mask

Tendency for cracks reduced (and dependent on mask design)

Cracks only perpendicular to stripes
ELOG II

Crack formation can be controlled by mask geometry

Cracks parallel to substrate in interface region
→ Route to spontaneous separation

Bow unchanged to planar growth

40 µm thick GaN on honeycomb mask (SIN)

Defect reduction in heteroepitaxy

Careful optimization of nucleation and buffer layer growth on sapphire or SiC
→ Mid \(10^7\) cm\(^{-2}\) dislocation density is possible
→ Still too high for laser diodes with high output power

Use of optimized substrate miscut: not well studied in literature

Increase layer thickness
→ Reduces defect density
→ Leaves problem of bow and cracks

Patterned growth / selective area growth
→ Reduces defect density
→ Can help with cracks
→ Leaves problem of bow
Freestanding GaN – Laser lift-off

Decomposition of GaN at interface

Stress from process + stress from epi ➔
high risk of cracking ➔ on 2” difficult

Used for substrate removal on chip level
(Thin GaN for high power LEDs)
➔ improved thermal management

Freestanding GaN – LiAlO₂

LiAlO₂ substrate decomposes at elevated temperature
➔ Freestanding layer after epi, no further process necessary

Layer quality to be improved

Promising route !!

Cooperation FBH - IKZ
Freestanding GaN - ELOG

Honeycomb mask with 5 µm windows and 15 µm spacing

WSiN mask

⇒ Decomposition of GaN, no sticking to mask
⇒ Separation during growth with little bow
⇒ Freestanding layer after epi, no further process necessary

Layer quality better than on LiAlO₂

Promising route for high quality seed wafers

K. Motoki et al., Jpn. JAP 40, L140 (2001)

Sumitomo: HVPE

ELOG on two sides of masked GaAs (111) ⇒ solves bow problem!
Locally dislocation density < 2x10⁶ cm⁻², homogeneity?
Announced for 2001, in 2003 20,000 € per piece, availability ??
Freestanding substrates from heteroepitaxy

Bowing and cracking need to be controlled

- solved by Sumitomo by growth on two sides
- solved by FBH by ELOG with WSiN mask
- optimization of process sequence (T cycles) on LiAlO₂

Too thin for defect reduction below 10⁶ cm⁻²

Nucleation process for each wafer → reproducibility?

No efficient multiwafer machines → too expensive?

→ Bulk growth probably the only way to get where we need to get

HVPE the only proven method with high growth rate →
Use epi method for bulk growth

Bulk growth by HVPE

2 – 3 mm long boules in 20 – 50 h
→ 5 substrates sawn from one boule

EPD down to 10⁶ cm⁻² at end of boule

In 2004 allotted in small quantities (numbered) for 10,000 € per 2”

Not to be used as seed layer!!

Now belongs to Cree, the SiC monopolist

→ It works but it needs to be made more efficient (and available)
Route to larger boules

Use experience with existing reactor and design new reactor suited for high thickness together with Aixtron

- Vertical $\Rightarrow$ no problem with convection
- Laminar flow over wide parameter range
- Reduced parasitic deposition, reaction concentrated to substrate area
- Good homogeneity at rates above 250 μm/h expected

We are looking forward to the results

Outlook

GaN substrates will be manufactured by HVPE

Short term:
- Laser diodes will be made on GaN substrates

Medium term:
- UV and green LEDs will most likely follow

Long term:
- HFETs with small feature size will be manufactured on large diameter Si:GaN (for research e-beam litho on SiC is o.k.)
- All GaN LEDs on GaN substrates?
Acknowledgement

Workshop organizers for invitation

Eberhard Richter for cooperation in preparing this talk and bringing HVPE forward

for funding project 01BU402

Project partners Aixtron, FCM, Osram, IAF, Uni Ulm for cooperation

Klaus Köhler (IAF) and Michael Heuken (Aixtron) for giving some input for this talk

The audience for your patience